C-RAN Employing xRAN Functional Split: Complexity Analysis for 5G NR Remote Radio Unit

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***Abstract*—Fronthaul (FH) bandwidth in cloud radio access network (C-RAN) can be significantly reduced with an appropriate functional split by offloading more signal processing functionalities to the remote radio unit (RRU). However, this not only reduces the acclaimed centralization benefits but also increases the complexity of the RRU. Considering the practical aspects such as power consumption, size, weight, it is often desirable to make RRU as simple, yet efficient, as possible. In this paper, we compute the computational requirement of the RRU with 5G New Radio (NR) considering functional split 7.2 as recently standardized split by the xRAN Forum. C-RAN with mix numerology allows to support a wide range of scenarios and use-case specific requirements. In addition, we compare suitability in terms of efficiency and flexibility of the RRU being implemented using either FPGA or GPP considering their computational requirement. Based on the complexity analysis, we calculate the required number of the FPGA or GPP to handle the complexity of the RRU. We show that FPGA is more feasible option compared to x86 in terms of form factor and power consumption particularly for rooftop mounted RRU.**

***Index Terms*—Cloud radio access network (C-RAN), Computational complexity, Functional split, FPGA,Gflops, GPP, xRAN**

I. Introduction

A plethora of new use cases and application scenarios such as enhanced mobile broadband (eMBB), ultra-reliable and low-latency communication (URLLC), and massive machine-type communication (mMTC) are envisioned in the fifth generation (5G) cellular systems, and they require a diverse set of requirements. 5G New Radio (NR) [1] brings the concept of the mix-numerology that allows to support mixed services with different waveform parameters, which is a key requirement in 5G. In addition, C-RAN and massive MIMO have been considered as promising technologies to meet these requirements.

Contrary to the conventional base station (BS) architecture, C-RAN [2] has a centralized signal processing entity, called base band unit (BBU), which is connected to the remotely located small form factor and low-powered base station, called remote radio unit (RRU). The BBU and RRU are connected by a high speed, low latency and highly reliable transport link known as fronthaul (FH), which forwards the digitized baseband IQ (in-phase and quadrature) samples to the BBU in uplink (UL) and to the RRU in downlink (DL) using commonly used common public radio interface (CPRI) [3] or eCPRI [4] standard. Despite the promising advantages of C-RAN such as improved spectral efficiency (SE) and energy efficiency (EE), and lower capital expenditure (CAPEX) and operating expenditure (OPEX) compared to conventional base station architectures, C-RAN suffers from stringent FH bandwidth, reliability, latency and jitter requirements [2].

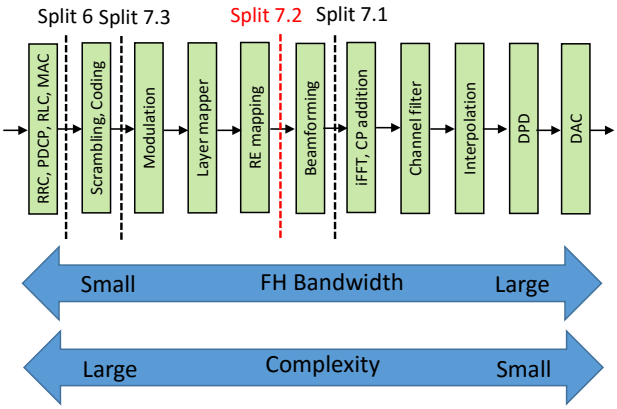

Fig. 1. xRAN Functional Split 7.2 showing full processing chain.

A. Functional Split

In order to relax the stringent FH requirements, functional splits between the BBU and RRU are defined [5], [6]. The functional split refers to a division of signal processing functionalities between the BBU and RRU. 3GPP [7] has identified eight functional splits with different suboptions. In addition, CPRI released a new version of CPRI called eCPRI [4], which already uses new splits. However, CPRI and eCPRI do not deliver a full interface standardization that would allow a true interoperability among different vendors. On the other hand, recently formed xRAN Fronthaul Working Group supports an open, interporable and efficient FH interface. xRAN has identified a single split point, known as 7.2x [8], and has delivered an extensive interface specification that will enable true interoperability between RRUs and BBUs of different vendors.

B. Motivation and Contribution

By offloading more signal processing functionalities to the RRU the required FH bandwidth is significantly decreased, which is desirable to lower the network deployment cost. However, it also reduces the acclaimed centralization coordinated multipoint benefits, and at the same time demands more processing power. Considering the practical implementation aspects, particularly the size, weight and power consumption, it is often desirable to keep the RRU as simple, yet efficient, as possible. In this paper, we compute the computational complexity of the RRU, especially in regards to the 5G NR mix-numerology when employing the xRAN functional split.

In centralized RAN processing, it is often assumed that general purpose processor (GPP) [9] e.g., x86 can be utilized, benefiting from economy of scale and pooling gains. In principle, all of the PHY layer functions can be performed on GPP hardware. However, future RATs employing e.g., carrier aggregation and mmWave communication with larger bandwidths, PHY processing will be challenging on GPP. Moreover, PHY layer processing functions are usually fixed, and require less flexibility or programmability. Hence, FPGAs or ASICS might be more suitable for use in the RRU.

Contribution: In this paper, our main contribution lies in finding out the computational requirement of the C-RAN focusing on the functional split 7.2 with detailed PHY functions being performed at the RRU shown in Fig. 1. In addition, we compute the requirements for 5G NR mix-numerology in order to account for different use cases and application scenarios. Further, for the offered computational requirement, we compare the deployment of the RRU using FPGA or GPP in terms of flexibility and power efficiency.

II. Mix-Numerology-based 5G NR

3GPP with Release 15 has finalized 5G NR specification [1] and it supports operation in wide range of frequency bands ranging from sub-1 GHz to mmWave bands. It has defined two frequency range (FR): FR1:450 MHz - 6 GHz (commonly referred to as sub-6) and FR2: 24.25 GHz - 52.6 GHz (also referred to as millimeter wave). In FR1 and FR2, the maximum bandwidth is 100 MHz and 400 MHz, respectively, which are much greater than the maximum LTE bandwidth of 20 MHz. In order to support a wide range of use cases and application scenarios, 5G NR supports flexible subcarrier spacing, which can be obtained using [1]:

$$\Delta f = 2^{\mu} \times 15 \text{ kHZ},$$

where $\mu \in \{-1, 0, 1, 2, 3, 4, 5\}$ is an integer. Accordingly, the slot duration is scaled by a factor of $T_{\text{slot}} = 2^{-\mu}$ compared to 1 ms LTE subframe duration, and each slot now contains 14[1] OFDM symbols. This means that the slot duration, T_{slot}, and hence, the cyclic prefix (CP) length, $T_{\text{CP}} = 2^{-\mu} \times 4.7\mu$s and OFDM symbol duration, $T_{\text{OFDM}} = 1/\Delta f$ reduces as the subcarrier spacing increases as illustrated in Fig. 2.

[1]It is to be noted that unlike LTE slot, which contains 7 OFDM symbols, a 5G NR slot contains 14 OFDM symbols.

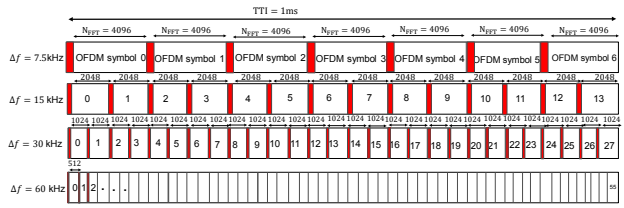

Fig. 2. Mix-numerology based frame structure

However, as only the sub-carriers within a numerology are orthogonal to each other, the sub-carriers from one numerology interfere with sub-carriers from neighbouring numerology causing inter-numerology interference (INI) [10]. Effect of INI can be mitigated e.g., by inserting guard tones between numerology [11] or by applying time-domain filtering per numerology (sub-band) or time-domain windowing [12]. It is claimed in [12] that windowing is an efficient and simple tool to control INI, and windowing has extremely low complexity, which, for simplicity, we ignored in our calculation.

A. Computational Complexity

The computational complexity of signal processing operations in literature is often stated in terms of giga operations per seconds (Gops). In this paper, we quantify the computational complexity in terms of the total number of real multiplications and real additions per symbol. We specify this in terms of giga flops (Gflops). The different stages of the signal processing functionalities block will have different complexities, hence depending upon the functional split being employed, the offered total complexity at the RRU will be different. Unlike the simple 3GPP functional block diagram, Fig.1 shows the C-RAN architecture with full processing chain showing detailed RF chain, which are important for practical implementation aspects. The necessary additions arise due to two main practical aspects [13], especially due to future RATS employing carrier aggregation and massive MIMO technologies. Firstly, the RRUs need to support several carriers at the same time, which requires digital channel filtering, up-conversion and carrier mixing to create a composite signal of many carriers. Secondly, in order to provide sufficient transmit power, RRUs have to use non-linear power amplifiers (PAs). In order to avoid distortion by non-linearity of the PAs, digital predistortion (DPD) needs to be applied. These processing steps significantly increase the required computational complexity and in this paper, we compute their complexity considering split 7.2. It is, in general, difficult to calculate the exact computational complexity as computational complexity of a certain function depends very much on the specific implementation. Nevertheless, based on the basic operation to be performed, order of magnitude can be estimated for comparison.

III. C-RAN Complexity Analysis

A. Computational Complexity for Beamforming

In order to compute the beamforming complexity, we consider a beamformer, which converts N_L data streams (layers/ beams) into N_{ant} antenna streams. For a given signal carrier bandwidth with $N_{\text{sub, act}}$ utilized subcarriers, and N_{sym} OFDM symbols per T_{sf} second, the output is produced at a rate of (samples/sec)

$$R_{\text{BF},L} = N_{\text{ant}} \cdot N_{\text{sub, act}} \cdot N_{\text{sym}} \cdot T_{\text{sf}}^{-1}. \quad (1)$$

One antenna sample corresponding N_L layers requires N_{CMA} complex multiplications and additions. Assuming that multiplications and additions can be performed within one clock cycle, and that one complex multiplication requires $N_{\text{OP, CMA}} = 3$ non-complex operations (flop), the total rate of operations can be obtained using:

$$R_{\text{BF, tot}} = R_{\text{BF},L} \cdot N_{\text{OP,CMA}} \cdot N_{\text{CMA}} \quad (2)$$

B. Mix-Numerology Integration and its Complexity Analysis

Computational complexity of mix-numerology based on the TTI frame structure is considered here. For this, we consider an example of 100 MHz bandwidth with and without mix-numerology configurations as shown in Fig. 3, where Fig. 3 (a) represents uniform division of the 100 MHz bandwidth into 5 different sub-bands 20 MHz each, and the FFT computation of the each sub-band is performed independently based on the TTI, Fig. 3 (b) represents non-uniform distributions of the 100 MHz bandwidth, and Fig. 3 (c) represents a full 100 MHz bandwidth with 15 kHz subcarrier spacing and FFT size of 8192[2].

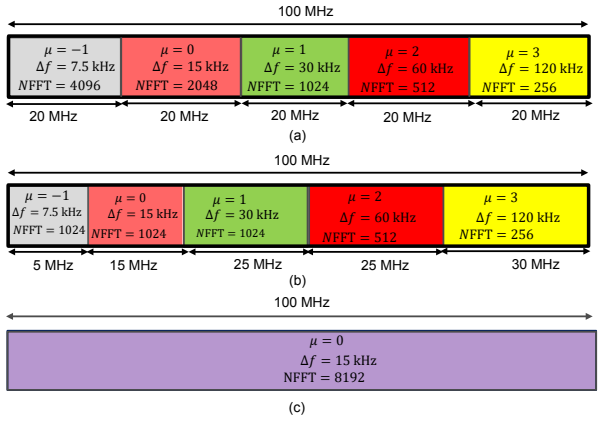

Fig. 3. FFT length calculation comparison of the 100 MHz bandwidth (a) Mix-numerology based on the uniform division of the bandwidth (b) Mix-numerology based on the non-uniform division of the bandwidth (c) Long FFT calculation based on the uniform subcarrier spacing of 15 kHz of 8192 FFT length

[2]Although in the standard, 100 MHz bandwidth with 15 kHz subcarrier spacing is not specified, we considered this spacing as a baseline since theoretical analysis is still valid.

After fixing FFT length of the each band based on the configurations shown in Fig. 3, goal is to compute the short FFT length of each band independently, However, after short FFT calculation, we have to perform first the interpolation and then mixing of the different frequency bands in order to match one of them with the same sampling rate as shown in Fig. 4. Therefore, the total complexity associated with mix-

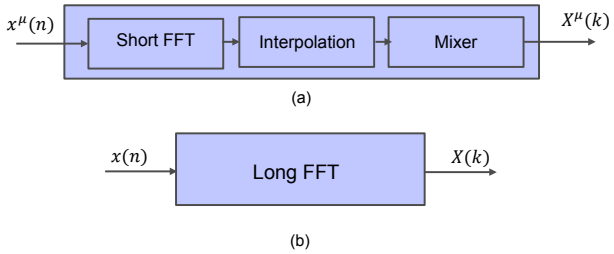

Fig. 4. Total computational complexity associated with mix-numerology of the short FFT length (a), where μ represent the different numerology, $x(n)$ and $X(k)$ denotes the time-domain and frequency-domain signal respectively (b) Long FFT

numerology can be obtained as

$$C_{\text{Total}} = C_{\text{FFT}} + C_{\text{interpolation}} + C_{\text{Mixer}}, \quad (3)$$

where C_{FFT} is complexity associated with FFT calculation and the detailed summary of the different efficient methods for computation of FFT is given in Table I, $C_{\text{interpolation}}$ is the complexity of the interpolation filter, and C_{Mixer} accounts for the complexity associated with the mixer that mixes different frequency bands. Now, considering the Fig. 4, we describe the

TABLE I: Different efficient methods for computation of FFT [14]- [15].

Complexity	Adder	Multiplier
DFT	$N_{\text{FFT}}(N_{\text{FFT}}-1)$	N_{FFT}^2
Radix-2	$N_{\text{FFT}}\log_2(N_{\text{FFT}})$	$\frac{N_{\text{FFT}}}{2}\log_2(N_{\text{FFT}})$
Split-radix algorithm	$3(N_{\text{FFT}}(\log_2(N_{\text{FFT}}) - 1) + 4)$	$N_{\text{FFT}}(\log_2(N_{\text{FFT}})-3)+4$
Sparse DFT	$k\log(n)\log(n/k))$	$k\log(n)\log(n/k))$

computation of associated complexity by the following steps [16]:

1) Complexity of N_{FFT} FFT can be computed in terms of number of addition and multiplication operations from Table I.
2) Insertion of the cyclic prefix (CP) on each sub-bands of the mix-numerology.
3) Complexity associated with low pass interpolation filter, whose filter length is approximately $N_{\text{FIR}}N_{\text{FFT}}/N$ is $N_{\text{FIR}}N_{\text{FFT}}(N_{\text{FFT}}+N_{\text{CP}})/N$, where N_{FIR} is the order of the filter required to match the output-sampling rate of 30.72 MHz, N_{FFT} is the required FFT length for each numerology, and N is the total FFT length for uniform subcarrier spacing.
4) Finally mixing at the output with the same sampling rate requires $N^{\mu}(N + N_{\text{CP}}N/N_{\text{FFT}})$ multiplications per

symbol, where N^{μ} is the total number of the numerology sub-bands.

C. Channel Filter

In order to model channel filter, we consider as an FIR filter based implementation of the channel. The total complexity of FIR filter is $C_{\text{FIR}} = C_{\text{FIR}}^{\text{Add}} + C_{\underset{\text{FIR}}{\text{Mult}}}$ flop, where

$$C_{\text{FIR}}^{\text{Add}} = P \times (N_{\text{FFT}} + N_{\text{cp}} - 1), \tag{4}$$

$$C_{\underset{\text{FIR}}{\text{Mult}}} = P \times (N_{\text{FFT}} + N_{\text{cp}}), \tag{5}$$

where P is the number FIR filter taps, and $N_{\text{FFT}} + N_{\text{cp}}$ is total number of input samples.

1) Digital Pre-Distortion (DPD): It is well known that PA causes non-linear distortions in the OFDM system. Due to this, OFDM system cause high peak-to-average power ratio (PAPR) and out-of-band (OOB) emission. In the literature, there are several techniques for linearization of the PA behaviour [17]. Among this, digital pre-distortion (DPD) is one of the most cost-effective linearization techniques. DPD adds an extra non-linear function before the PA to process the input signal. Therefore, resulting cascade (DPD+PA) behaviour is linear [17]. For K^{th} order, DPD filter complexity is $4KQN_{\text{ant}}$ flop [17], where Q the memory depth, and N_{ant} the number of transmit antennas in the DL. The DPD complexity can be obtained as $C_{\text{DPD}} = C_{\text{DPD}}^{\text{Add}} + C_{\underset{\text{DPD}}{\text{Mult}}}$ flop, where

$$C_{\text{DPD}}^{\text{Add}} = (N_{\text{FFT}} + N_{\text{cp}} - 1) \times 4 \times K \times N_{\text{ant}}, \tag{6}$$

$$C_{\text{DPD}}^{\text{Mult}} = (N_{\text{FFT}} + N_{\text{cp}}) \times 4 \times K \times N_{\text{ant}}. \tag{7}$$

IV. Results

The computational complexity is measured in terms of floating point operations per second (FLOPS). Depending on the processor characteristics, every function of Fig.1 can show different computational complexity for different processor. The required computational power has to be computed and compared into relation with the one available from different platforms. As an example, for FPGA processing, we use a Xilinx Ultrascale+ [18] and for GPP, we use Xeon 6140 [19] as a reference.

A. Xilinx FPGA

A Xilinx ultrascale FPGA features $N_{\text{DSP}} = 4272$ DSP48s, which can perform one operation each and can run approximately up to $C_{\text{FPGA}} = 500$ MHz. However, usually an FPGA cannot utilise all resources at maximum clock speed, so assuming a maximum utilization of $\mu_{\text{FPGA}} = 0.7$, the total computational power is estimated as

$$\begin{aligned} R_{\text{FPGA}} &= N_{\text{DSP}} \cdot C_{\text{FPGA}} \cdot \mu_{\text{FPGA}} \\ &= 1495 \text{ Gops}. \end{aligned} \tag{8}$$

Power consumption of FPGAs is not straight forward, as it usually depends on many factors like the overall utilisation. From [18], we estimate a typical FPGA power consumption as $P_{\text{FPGA}} = 30$ W.

B. Xeon 6140

Xeon 6140 is a version of GPP, which features up to $N_{\text{cores}} = 18$ cores, each core can perform $N_{\text{flop}} = 32$ flops per cycle and it runs at a maximum clock speed of $C_{\text{xeon}} = 2.6$ GHz. Assuming a processor utilization of $\mu_{\text{xeon}} = 0.7$, total computational power can be calculated as

$$\begin{aligned} R_{\text{xeon}} &= N_{\text{cores}} \cdot C_{\text{xeon}} \cdot N_{\text{flop}} \cdot \mu_{\text{xeon}} \\ &= 1048 \text{ Gflops}. \end{aligned} \tag{9}$$

The power consumption of Xeon 6140 is approximately $P_{\text{xeon}} = 140$ W.

C. Mix-Numerology Complexity Analysis

Here, our goal is to compute and compare complexity between the different mix-numerology. Fig.5 shows complexity association with 100 MHZ bandwidth, where 100 MHz bandwidth is equally split into 5 different sub-bands each of the 20 MHz (refer Fig. 3(a)). The same color corresponding to individual sub-band is used to show their corresponding complexity. We can see that complexity of sum of all individual sub-bands, denoted by $\sum C_{\mu}^{\text{uniform}}$, is comparable to the that of a single 100 MHz band, denoted by $C_{\text{100 MHz}}^{\Delta f=15\ kHz}$.

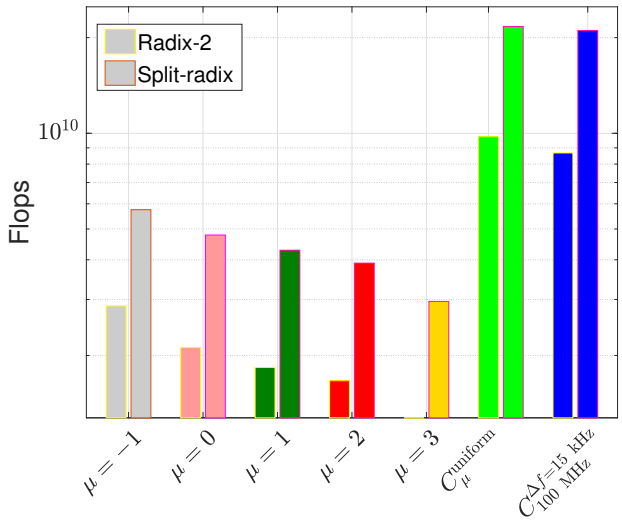

Fig. 5. Complexity comparison between uniform subcarrier spacing as given in Fig. 3 (a) and long FFT calculation

Similarly, Fig. 6 shows complexity of each sub-bands when 100 MHz band into the non-uniformly as shown in Fig.3(b). Unlike in uniform bandwidth division case, in non-uniform bandwidth division, the sum of all individual complexity, denoted by $\sum C_{\mu}^{\text{non-uniform}}$ is less as compared to that from 3 (c).

D. Computational Complexity for Beamforming

As explained in Sec. III-A, the beam forming complexity depends on the available subcarriers, which in turn depends

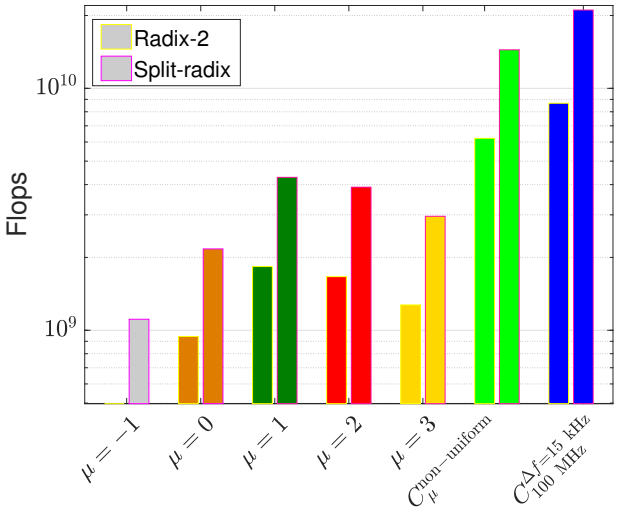

Fig. 6. Complexity comparison between non-uniform subcarrier spacing as given in Fig. 3 (b) and long FFT calculation

on the carrier aggregation bandwidth. Fig. 7 shows beamforming complexity for different carrier aggregation technologies for four antenna numbers. It is obvious that beamforming complexity increases with the antennas at the RRU and carrier signal bandwidth.

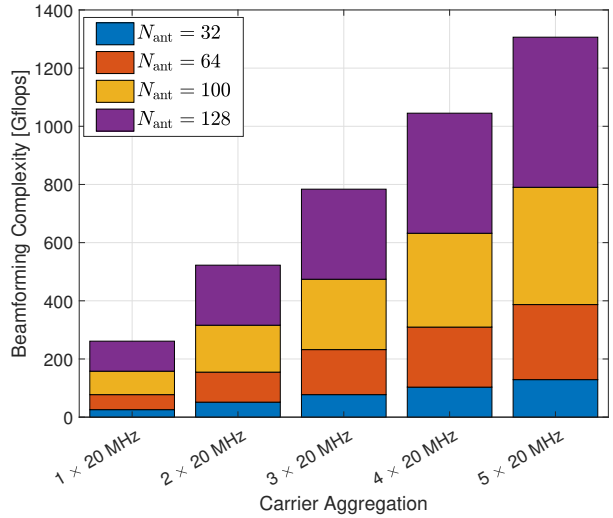

Fig. 7. Beam forming complexity for different carrier aggregation

Figure 8 shows individual complexity of each block based on the Split 7.2. By following the LTE specification, we consider complexity calculation of the channel filter based on FIR filter with $P = 81$ paths. Similarly, complexity calculation of the DPD filter is also based on the FIR filter, but we consider the $K = 4^{\text{th}}$ order filter with $N_{\text{ant}} = 64$ antenna ports.From the Fig. 8, is is clearly visible that DPD consume most of the computation. This arises mainly due to more processing involved in compensating the non-linear distortion of the PA for making PA to operate in linear region.

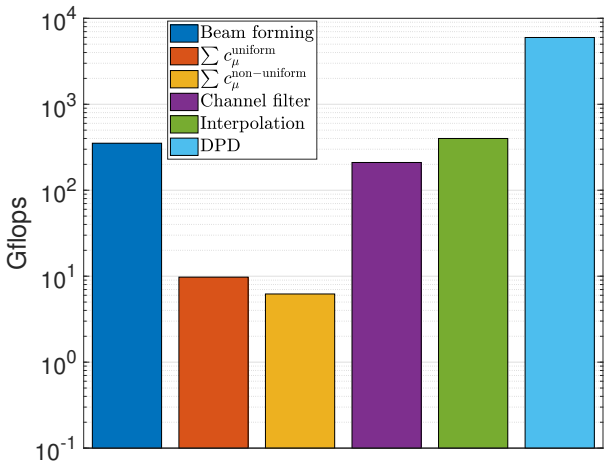

Fig. 8. The individual complexity calculation for the each part of the DL that need to consider into the 7.2x splits

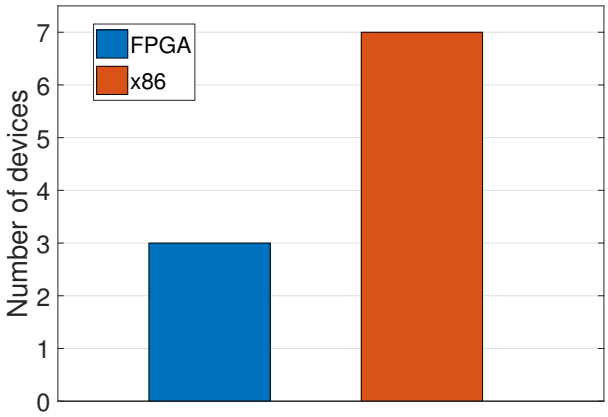

Fig. 9. Number of device required

Figure 9 shows about the required number of the FPGA or x86 devices based on the total complexity calculation given in the Fig. 8. The number of required devices can be calculated by

$$N_{\text{FPGA/Xeon}} = C_{\text{total}}/R_{\text{FPGA/Xeon}}, \tag{10}$$

where C_{total} is the the total complexity by signal processing chain and $R_{\text{FPGA/Xeon}}$ refers to the rate of FPGA or GPP in Sec. IV. A and B. We see that it requires three FPGA devices and about seven x86 devices for 100 MHz bandwidth. The corresponding power of FPGA would be 90 W and that of Xeon would be 980 W. From this calculation, it can be concluded that FPGAs are only the feasible option, especially considering the form factor and power consumption. On the other hand, we need $7 \times 18 = 126$ Xeon x86 cores correspond to a powerful data center of 7 Xeon devices, which is not feasible for a rooftop mounted RRU. Although we computed the required number of devices for 100 MHz bandwidth, similar process can be repeated for any other bandwidth. It is to be, however, noted that these number gives only the practical

insights for comparison as actual number of required device will be different depending upon the advancement of the future technologies, especially due to less power consumption and more efficient computational capabilities.

V. Conclusion

In this paper, we considered complexity analysis of the xRAN fictional split 7.2 based on the 5G NR. We considered complexity analysis with full signal processing chain. We also presented complexity associated with different numerology's for both uniform and non-uniform bandwidth division, and finally compared total complexity of mix-numerology with complexity associated with of a single 100 MHz with 15kHz sub-carrier spacing. In addition, based on the total complexity, we estimated the required number of FPGA or GPP for RRU. We showed that FPGA is more feasible option, especially in terms of RRU form factor and power consumption compared Xeon x86 processors. Moreover, we found that the most signal processing entity is DPD.

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