Compute Resource Disaggregation: An Enabler for Efficient 5G RAN Softwarisation

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***Abstract*—This paper proposes the concept of compute resource disaggregation in centralized softwarised Radio Access Networks. This approach allows individual allocation of processing functions, to different servers depending on the nature and volume of their processing requirements. The benefits of the proposed approach are evaluated through experiments analyzing the BBU processing requirements of LTE using an open source suite for wireless systems and a purposely developed Multistage Linear Programming modeling framework. Our results show significant benefits of the proposed approach compared to the traditional solution in terms of energy efficiency.**

Keywords*— *RAN; BBU; softwarised radio; compute disaggregation; multistage linear programming.

I. INTRODUCTION

The increase of mobile traffic predicted in 5G networks as well as the wireless access technology densification and technology advancements proposed to address this, introduce very stringent requirements in the Radio Access Networks (RANs). Traditional distributed RAN solutions, where Base Band Units (BBUs) and radio units (RUs) are co-located, suffer several limitations. To overcome these limitations Cloud Radio Access Networks (C-RANs) have been proposed. In C-RAN, distributed Remote Radio Heads (RRHs) are connected to a BBU pool, the Central Unit (CU), through high bandwidth transport links known as fronthaul (FH). The CU can be hosted in data centers (DCs) comprising General Purpose Processors (GPPs) that can be accessed through FH services supported by the transport network of the 5G infrastructure [1]. The interface between RUs and CU is standardized through the Common Public Radio Interface (CPRI).

In this environment it is very important to identify the optimal allocation of BBU functions to the appropriate servers hosted by the CU, as it is expected to give significant efficiency gains. To the best of the authors knowledge, up to date, this is performed without taking into consideration the details and specificities of the individual processing functions that BBUs entail. To take advantage of the appropriate mapping of processing functions to suitable available compute resources within the CU we propose, for the first time, the concept of compute resource disaggregation. This approach allows individual allocation of processing functions, associated with a specific FH service, to different servers depending on the nature and volume of their processing requirements. To quantify the benefits of the proposed approach we have performed experiments analyzing the BBU processing requirement of LTE using an open source suite for benchmarking wireless systems (WiBench) [2]. In addition, a Multistage Integer Linear Programming (ILP) modeling framework was developed able to assign the construction elements of the BBU chain to the suitable servers hosted by the CU. The output of our experiments was used as a realistic input to our ILP model in order to evaluate the energy consumption requirements of the compute resources for the proposed and the traditional Softwarised BBU (SW-BBU) approach [3]. As the proposed approach is based on the concept of disaggregation we refer to it as the disaggregated SW-BBU (DSW-BBU) approach. Our results show that the proposed DSW-BBU approach can provide significant benefits in terms of energy consumption and as such operational expenditure associated with the BBU functions.

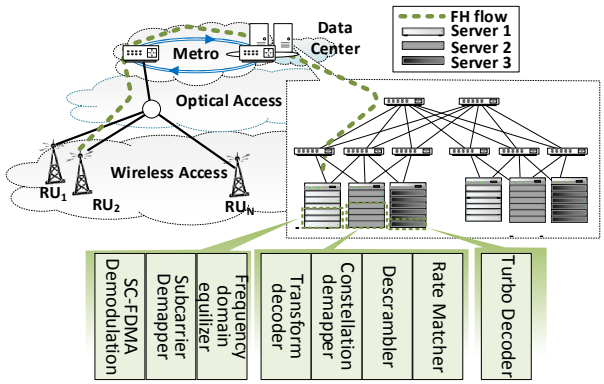

Figure 1: Centralized processing of softwarised-RAN functions on a data center hosting different type of servers.

II. PROBLEM STATEMENT

We consider a generic 5G C-RAN where the processing requirements of a set $\mathcal{R}$ of R RRHs is supported by a set of compute resources located at the CU. The compute resources comprise a set S of GPPs with each processor having processing capacity C_s and performance per watt (measured in Instructions per Second - IPS) P_s. Servers are organized following the simple tree structure of Figure 1 and are responsible to provide the necessary compute power for the provisioning of FH services. This is achieved through the execution of baseband signal processing related tasks in support of the RRHs' operation. The compute requirements for baseband processing for RU $r, r \in \mathcal{R}$, can be calculated by the sum of all contributing computing elements responsible to perform the required functions including, Single Carrier - Frequency Division Multiple Access (SC-FDMA) Demodulation (c_{r1}), Subcarrier

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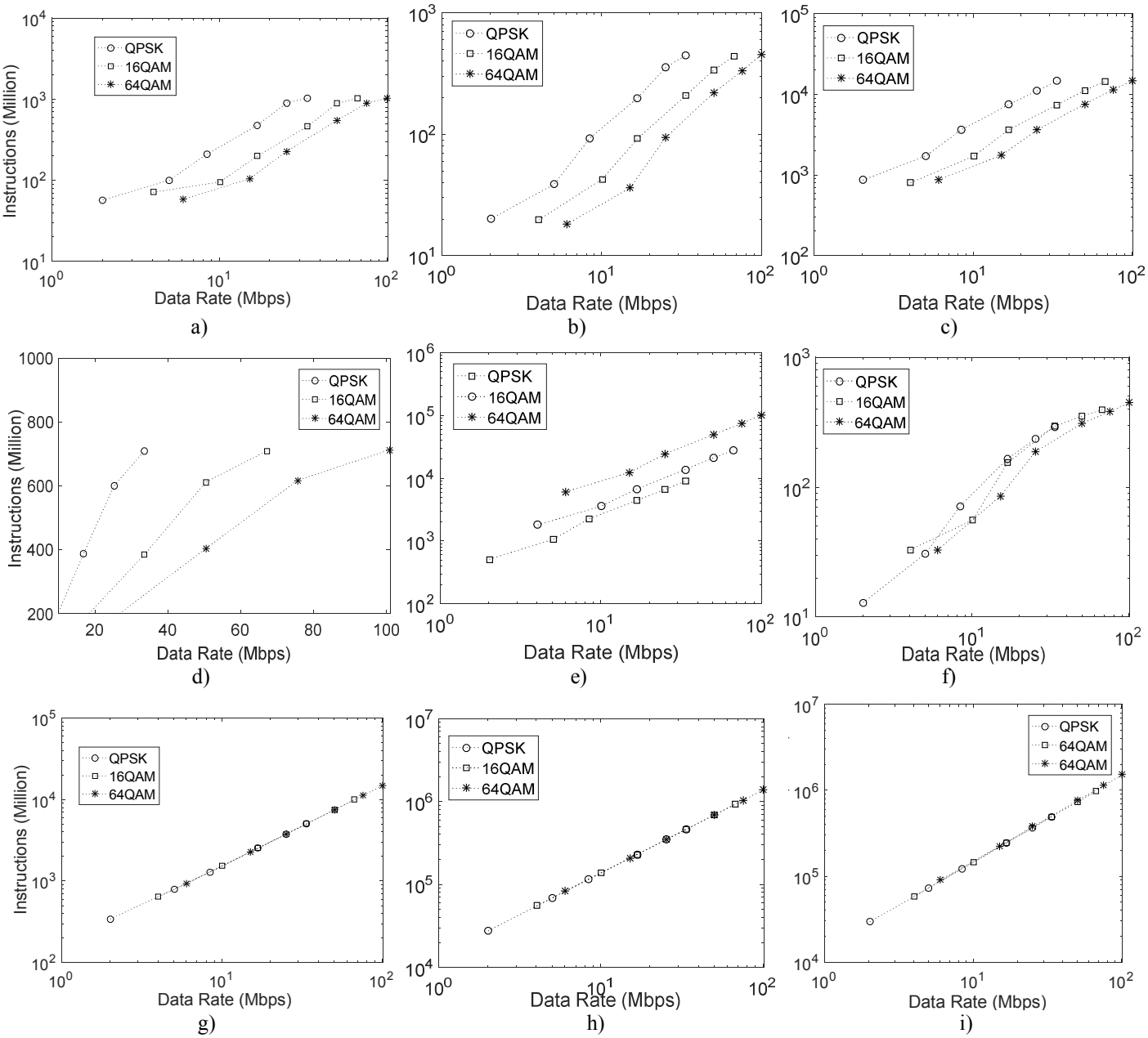

Figure. 2: Instructions per signal processing function under various data rates for a) SC-FDMA Demodulation, b) Subcarrier Demapper, c) Equalizer, d) Transform Decoder, e) Demodulation, f) Descrambler, g) Rate Matcher, h) Turbo Decoder, and i) Total Instructions.

Demapper (c_{r2}), Frequency Domain Equalizer (c_{r3}), Transform Decoder (c_{r4}), Constellation Demapper (c_{r5}), Descrambler (c_{r6}), Rate Matcher (c_{r7}) and Turbo Decoder (c_{r8}). As shown in Figure 1, these functions need to be executed in a specific order.

The main objective of this work is to identify the optimal GPP server where each function can be allocated so the total power consumption at the DC can be minimized satisfying, at the same time, the strict Quality of Service (QoS) constraints imposed by the CPRI protocol. To achieve this, we initially calculate - in terms of Total Instructions - the actual processing requirements of each baseband processing function under various wireless access system configurations. These calculations are carried out using WiBench, an open source software implementation of the LTE protocol stack [2]. The processing requirements of each function are then used as input to a multistage ILP-based optimization framework that is able to assign each baseband sub-task to the suitable GPP in an energy efficient manner. Although the problem of BBU placement has been studied by several authors [4]-[7], the vast majority of these consider the BBU chain as a whole, without considering the specificities of its individual construction elements. In this study, however, it is shown that by i) *disaggregating* the softwarised BBU into a set of smaller sub-tasks, ii) *analyzing in depth the computational requirements* of each subtask and iii) *allocating* these subtasks to suitable GPPs as appropriate, significant benefits in terms of the operation efficiency of future 5G

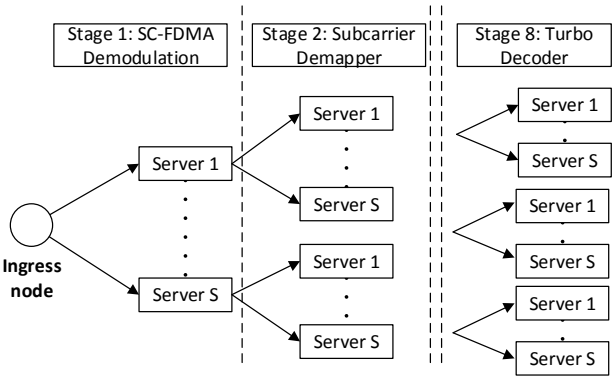

Figure. 3: Multi-stage optimization of disaggregated RAN functions

systems can be achieved. This study extends the state-of-the-art through:

- an extensive set of experiments used to characterize the processing requirements of the baseband functions as a function of the operational parameters of the wireless access network. These experiments led to the extraction of simple mathematical relations that can be used by network designers and operators to optimally allocate and size DC networks under various 5G network operational conditions.
- the development of an energy-aware multistage ILP-based optimization framework able to assign the BBU subtasks to a heterogeneous set of GPP elements reducing the DC power consumption by 20%.

III. BENCHMARKING FRAMEWORK

A. Experimental Platform Description

For our experiments we used WiBench, an open source suite for benchmarking wireless systems, and Intel's VTune Amplifier 2018, a performance profiler for software performance analysis. WiBench provides various signal processing kernels. These kernels are configurable and can be used to build applications to model wireless protocols. The LTE uplink that was used for the experiments, was provided by the WiBench suite and VTune was used to profile the LTE application. A summary of the functions that the BBU processing comprises is presented below. This includes:

- The Single Carrier - Frequency Diversity Multiple Access is a precoded Orthogonal Frequency Diversity Multiplexing (OFDM). It is preferred over OFDM, for the uplink transmission, because it is less susceptible to frequency offsets and has a lower Peak-to-Average Power Ratio. The SC-FDMA Demodulation function removes the Cyclic Prefix (CP) and performs N-point FFT.
- The Sub-carrier Demapper that extracts the data and the reference symbols from the subframes.
- The Frequency Domain Equalizer that estimates the Channel State Information (CSI) by the received pilot signal through the Least Square estimation algorithm. It computes the channel coefficients, with the help of CSI, and equalizes the received data using as equalizer a zero forcing MIMO detector in the frequency domain.
- The Transform Decoder that performs M-point Inverse Fast Fourier Transfer (IFFT).
- The Constellation Demapper that receives the signal and extracts the binary stream by generating Logarithmic Likelihood Ratios (LLR).
- The Descrambler that descrambles the input sequence.
- The Rate Matcher that separates the input stream into R, where R is the Channel Code Rate, de-interleaves each code stream and removes redundant bits. For our experiments R was constantly set to 3.
- The Turbo Decoder that takes soft information for each code, in our case LLR, and it applies iterative the Soft-Input Soft-Output (SISO) algorithm. The Turbo Decoder consists of two SISO decoders that perform the trellis traversal algorithm, and one interleaver/deinterleaver. A higher number of iterations leads to a higher computation cost but achieves improved error correction performance. For all the experiments that were conducted the number of iterations was set to 5.

B. Main Results

To increase the statistical validity of the results produced by the profiler, a high number of iterations were performed (1000 subframes). The set of experiments we carried out was aiming at exploring the behavior of each processing function for different configurations of the LTE uplink system. In Figure. 2 we present the instructions performed, in order to process 1000 subframes, by each function as a function of the data rate for different modulation schemes.

Taking into consideration the variance of the measurements we can conclude that all functions present a linear dependence with the data rate. On the other hand, the influence of the modulation scheme, on the instructions number, differs for each function. More specifically we observe that the modulation scheme does not affect the instructions number for SC-FDMA Demodulation, Sub-carrier Demapper, Equalizer, and Transform Decoder. For the Constellation Demapper an exponential dependence of the modulation scheme is observed, while the Rate Matcher and the Turbo Decoder exhibit linear dependence.

We observe that the Turbo Decoder performs higher number of instructions, especially as the data rate increases, while the Constellation Demapper, the Rate Matcher and the Equalizer perform fewer instructions. This means that the Turbo Decoder, involving 1 to 4 orders of magnitude more instructions compared to other functions, determines by large the total number of instructions needed to process a subframe and how this number depends on the data rate and the modulation scheme.

TABLE 1: TECHNICAL SPECIFICATIONS OF THE SERVERS USED IN THE NUMERICAL EVALUATIONS

Enclosure (if applicable)	CPU Description	MHz	Chips	Cores	Total	RAM (GB)	Max IPS	Max Power (Watt)	Idle (Watt)	(IPS/watt)
QuantaGrid S31A-1U	Intel E3-1260L v5	2900	1	4	8	16	31802689	47.9	14.4	529836
QuantaGrid D51B-2U	Intel Xeon E5-2699 v4	2200	2	44	88	64	226542946	247	46.6	775056
QuantaGrid D52BQ-2U	Intel Xeon Platinum 8180	2500	2	56	112	192	378651974	426	39.5	833346
QuantaGrid T42S-2U	Intel Xeon Platinum 8176	2100	8	224	448	768	1304763025	1478	206	766748

IV. OPTIMIZATION OF SOFTWARIZED RAN FUNCTIONS

A. Problem formulation

Once the computational requirements $c_{\mathrm{ri}}, i = 1,\ldots,8$, of the dissagregated RAN functions for RU $r \in \mathcal{R}$ have been determined (Figure. 2), a multi-stage ILP modeling framework able to assign the construction elements of the BBU chain to the suitable servers, is proposed. During stage 1, the first function of all fronthaul flows in the service chain (i.e., function SC-FDMA Demodulation) reaching the CU will be assigned to servers $s \in$ S. This is achieved by minimizing the total compute resource power consumption, approximated through the following cost function:

$$f_1(\mathbf{x}_1) = \sum_{s\in S} \mathcal{E}_s \left(\sum_{r\in R} x_{rs1} c_{r1} \right) \quad (1)$$

In (1), the summation $\sum_{r\in\mathcal{R}} x_{rs1} c_{r1}$ captures the total processing load of all c_{r1} functions processed at server s, x_{rs1} is a binary decision variable indicating whether function c_{r1} of RU $r \in \mathcal{R}$ is processed at server s or not, $\mathbf{x}_1$ is a vector containing all first stage decision variables x_{rs1} and $\mathcal{E}_s$ is the power consumption model of server s.

Now let $Q_{\mathcal{R}1}$ be a set of paths for the FH flow of RU $r, r \in \mathcal{R}$ interconnecting the ingress node to server s, z_{rq} be the network capacity allocated to path $q \in Q_{\mathcal{R}1}$ for flow r and h_{r1} the transport network bandwidth requirements of function c_{r1}. h_{r1} can be directly estimated using the analysis [8]. (1) should be minimized subject to a set of network and processing demand constraints described through the following set of equations:

$$\sum_{s\in \mathrm{S}} x_{rs1} = 1, \qquad \forall\, r \in \mathcal{R} \ (2)$$

$$\sum_{r\in\mathcal{R}} x_{rs1} c_{r1} \le C_{s1}, \qquad \forall\, s \in S \ (3)$$

$$\sum_{s\in S} \sum_{q\in Q_{\mathcal{R}1}} x_{rs1} z_{rq} = h_{r1}, \forall\, r \in \mathcal{R} \ (4)$$

$$\sum_{r\in\mathcal{R}} \sum_{s\in S} \sum_{q\in Q_{\mathcal{R}1}} \delta_{rqe} z_{rq} \le C_{e1}, \forall\, e \in E \ (5)$$

Constraint (2) limits the number of servers where c_{r1}-type of functions can be processed to one, (3) indicates that the total number of tasks that can be assigned to server $s, s \in S$ cannot exceed its available processing capacity C_{s1} at stage 1, while equations (4) - (5) introduce network demand and capacity constraints, respectively. In (5), δ_{rqe} is a binary coefficient taking values equal to 1 if e belongs to path $q \in Q_{R1}$ realizing demand c_{r1}d at server s and C_{e1} is the available capacity of network link e at stage 1. After the solution of the first stage optimization problem, the remaining server and network capacity that can be used for the subsequent functions in the chain will be equal to:

$$C_{s1} - \sum_{r\in R} x_{rs1} c_{r1} = C_{s2} \ (6.1)$$

$$C_{e1} - \sum_{r\in\mathcal{R}} \sum_{s\in S} \sum_{q\in Q_{\mathcal{R}1}} \delta_{rqe} z_{rq} = C_{e2} \ (6.2)$$

The decision variables x_{rs2} of the second stage optimization problem responsible to forward (through a set of candidate paths $q \in Q_{\mathcal{R}2}$) and allocate the second function of the FH service chain ($c_{r2} \equiv$ subcarrier demapper) to the optimal server s for processing, depends on the results of the first stage problem. Typical example incudes the lists of paths Q_{R2} that can be used to forward the output of the first function in the chain to the subsequent one (i.e., c_{r1} to c_{r2}). This set depends on the decisions taken by the first stage problem regarding the servers where c_{r1} functions can be placed. Other examples include the available capacity at the servers and network links. All this unknown information captured through data vectors $\xi_t, t = 2,..,8$, is revealed gradually as we proceed deeper in the processing of the service chain. The optimal compute resource assignment problem in disaggregated RAN environments can be solved through the minimization of the following nested cost function:

$$\min_{\mathbf{x}_1\in\mathcal{X}_1} f_1(\mathbf{x}_1) + \mathbb{E}\left[\inf_{\mathbf{x}_2\in\mathcal{X}_{2(\mathbf{x}_1,\xi_2)}} f_2(\mathbf{x}_2,\xi_2) + \mathbb{E}\left[\cdots + \mathbb{E}\left[\inf_{\mathbf{x}_8\in\mathcal{X}_{8(\mathbf{x}_7,\xi_8)}} f_8(\mathbf{x}_8,\xi_8) \right]\right]\right] \quad (7)$$

where extending (1) $f_t(\mathbf{x}_t,\xi_t) = \sum_{s\in S} \mathcal{E}_s\left(\sum_{r\in R} x_{rst} c_{rt}\right)$, $\xi_t = (C_{st}, C_{et}, h_{rt}, z_{rq},)$ and based on (2)-(6) $\mathcal{X}_t$, $t = 2,..,8$, can be described through:

$$\mathcal{X}_t := \Bigg\{ \mathbf{x}_t : \sum_{s\in \mathrm{S}} x_{rst} = 1, \sum_{r\in R} x_{rst} c_{rt} \le C_{st}, \sum_{s\in S} \sum_{q\in Q_{Rt}} x_{rst} z_{rq} = h_{rt}, \sum_{r\in\mathcal{R}} \sum_{s\in S} \sum_{q\in Q_{Rt}} \delta_{rqe} z_{rq} \le C_{et}, C_{st-1} - \sum_{r\in R} x_{rst-1} c_{rt-1} = C_{st} \quad C_{et-1} - \sum_{r\in\mathcal{R}} \sum_{s\in S} \sum_{q\in Q_{Rt-1}} \delta_{rqe} z_{rq} = C_{et} \Bigg\}$$

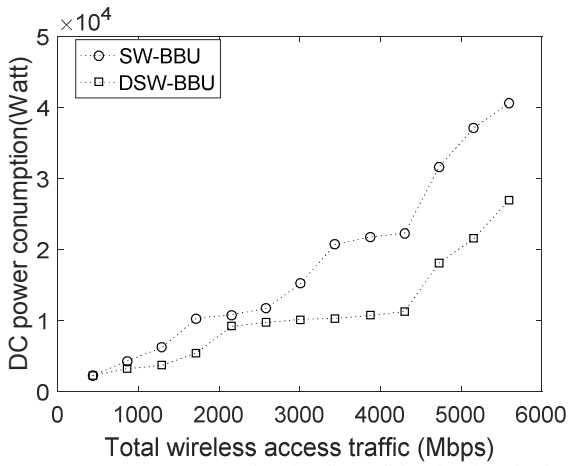

Figure. 4: DC power consumption for the traditional softwarised BBU (SW-BBB) and the disaggregated SW-BBU (DSW-BBU) as a function of the total wireless access traffic.

The multi-stage linear programming model (7) can be decomposed into simpler sub-problems using the duality theory [9].

B. Numerical results

To quantify the benefits of the proposed Softwarised RAN approach, the simple DC network topology of Figure 1 is considered. This topology comprises 6 racks each one packed with 48 servers. Connectivity between racks is provided with the switching solution provided in [10]. In the numerical calculations we consider four types of servers, randomly placed inside the racks. The technical specifications of these servers is provided in Table 1, while their power consumption follows the linear stepwise function described in [11]. For the wireless access, we consider the topology described in [1] in which the served area is covered by a set of RRHs who forward their FH flows to the DCs for processing. Given that this study focuses on the computational aspects of the FH flows, we make the rational assumption that the transport network does not act as a bottleneck and, the same time, it has sufficient capacity to transfer all flows to the DCs for processing.

Figure. 4 compares the performance of the proposed optimization scheme (denoted as Disaggregated Softwarised BBU – DSW-BBU) in terms of power consumption with the traditional Softwarised BBU (SW-BBU) as a function of the served traffic. As expected, the power consumption at the DCs increases with the wireless access load. However, the DSW-BBU offers much better performance due to its increased ability to mix and match compute and network resources, leading to improved utilization of the servers and to higher energy efficiency.

V. CONCLUSIONS

In this paper our experimental results show that there are specific functions (Turbo Decoder, Constellation Demapping, Rate Matcher and Frequency Domain Equalizer) at the LTE uplink that introduce much higher demands in terms of computational resources. For these functions, the number of instructions executed has a linear dependence of the data rate. Since the baseband processing workload can be split into several functions, the allocation of each function to a suitable server using a purposely developed multistage optimization framework, in the scenario of a heterogeneous DC, can lead to better utilization of the servers and to higher energy efficiency.

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